CLAIMS

What is claimed is:

1. A method of forming a contact to a source/drain contact region of a transistor device having a gate and the source/drain contact region is comprised substantially of a first material, the method comprising:

implanting particles including atoms having an atomic radius larger than an atomic radius of the atoms of the first material into a region of the source/drain contact region;

activating the atoms of the particles implanted into the source/drain contact region;

implanting a source/drain dopant into the source/drain contact, wherein the implanting the source/drain dopant is performed subsequent to the activating the atoms;

forming a metal silicide over the source/drain contact region after the activating to form the contact.

2. The method of claim 1 wherein the activating the atoms further includes activating the atoms in order to make the atoms substitutional in a lattice of the source/drain contact region, wherein the lattice includes atoms of the first material.

3. The method of claim 1 wherein the activating the atoms increases a lattice constant of the lattice in the source/drain contact region.

4. The method of claim 1 wherein the first material is silicon.

5. The method of claim 4 wherein the atoms implanted include germanium atoms.

6. The method of claim 1 wherein the atoms implanted include germanium atoms.

7. The method of claim 1 wherein the activating includes heating the source/drain contact region to a temperature of greater than 550 C.

8. The method of claim 1 wherein the activating includes heating the source/drain contact region to a temperature of greater than 1000 C.

9. The method of claim 1 wherein the activating further includes heating the source/drain contact region to a temperature in a range of approximately 900 – 1400 C.

10. The method of claim 1 wherein the activating further includes rapid thermal annealing of the source/drain contact region.

11. The method of claim 1 wherein the activating further includes laser annealing of the source/drain contact region.

12. The method of claim 1 wherein the activating further includes arc lamp thermal annealing of the source/drain contact region.

13. The method of claim 1 wherein the activating further includes gas convection annealing of the source/drain contact region.

14. The method of claim 1 wherein the implanting the particles is performed at a temperature between 25 and 600 degrees Celsius.

15. The method of claim 1 wherein the metal silicide is characterized as nickel silicide.

16. The method of claim 1 wherein the metal silicide is characterized as cobalt silicide.

17. The method of claim 1 further comprising:
forming a sidewall spacer adjacent to a sidewall of the gate, wherein the implanting the particles is performed prior to the forming the sidewall spacer.

18. The method of claim 17 wherein the forming the sidewall spacer is performed prior to the implanting the source/drain dopant.

19. The method of claim 1 wherein the gate is over a semiconductor substrate, the source/drain contact region is in the semiconductor substrate, and the source/drain contact region is disposed laterally from the gate.

20. The method of claim 19 further comprising implanting a second source/drain dopant in the semiconductor substrate after the implanting the source/drain dopant, wherein the second source/drain dopant is implanted deeper than the source/drain dopant.

21. The method of claim 19 wherein the implanting the particles further includes implanting with an energy of at least 3 keV.

22. The method of claim 19 wherein the implanting the particles further includes implanting with an energy in the range of 3 keV to 50 keV.

23. The method of claim 19 wherein the implanting the particles further includes implanting at a dose of at least 1E13 atoms per centimeter squared.

24. The method of claim 19 wherein the implanting the particles further includes implanting at a dose in the range of 1E13 to 1E17 atoms per centimeter squared.

25. The method of claim 19 wherein the implanting the particles is performed at a temperature between 25 and 600 degrees Celsius.

26. The method of claim 1, wherein:

the transistor has a second source/drain contact;

the implanting of the particles further includes implanting the particles into the second source/drain contact region;

the activating of the atoms further includes activating the atoms of the particles implanted into the second source/drain contact region; and

the implanting of the source/drain dopant further includes implanting the source/drain dopant into the second source/drain contact region;

further comprising forming a second metal silicide over the second region to form a second contact.

27. The method of claim 1 wherein the source/drain dopant includes boron.

28. The method of claim 1, wherein the gate is over a semiconductor substrate and a channel is in the substrate under the gate, further comprising forming a source/drain extension adjacent to the channel in the semiconductor substrate.

29. The method of claim 28 wherein the particles include ions, wherein the ions include the atoms.

30. The method of claim 28, wherein the forming comprises:

implanting a second source/drain dopant into the substrate for forming the source/drain extension, wherein the implanting the second source/drain dopant is performed prior to the implanting the source/drain dopant.

31. The method of claim 1 further comprising activating the source/drain dopant.

32. The method of claim 1, wherein the particles including atoms comprises only one of germanium, gallium, arsenic, indium, tin, antimony, thallium, lead, bismuth, zinc, cadmium, mercury, selenium, tellurium, and polonium.

33. The method of claim 1, wherein the particles including atoms comprises at least one of gallium, arsenic, indium, tin, antimony, thallium, lead, bismuth, zinc, cadmium, mercury, selenium, tellurium, germanium, and polonium

34. A method of forming a semiconductor device, the method comprising:

implanting particles into a region of a substrate, the substrate containing atoms of a first material, the particles including

atoms having an atomic radius larger than an atomic radius of the atoms of the first material;

activating the atoms implanted into the region of the substrate with a non diffusion activation process; and

forming a metal silicide over the second region after the activating.

35. The method of claim 34 wherein the non diffusion activation process includes one of arc lamp rapid thermal annealing of the region and laser annealing of the region.

36. A method of forming a semiconductor device, the method comprising:

forming a gate over a semiconductor substrate, the substrate having a lattice having a lattice constant;

increasing the lattice constant of the lattice in a region of the substrate after the forming the gate;

implanting a source/drain dopant into the substrate for forming at least a portion of a source/drain region in the substrate, wherein the implanting the source/drain dopant is performed subsequent to the increasing the lattice constant;

forming a metal silicide over the portion of the region.

37. The method of claim 36 wherein the first material is silicon.

38. The method of claim 36 wherein the metal silicide is characterized as nickel silicide.

39. The method of claim 36 wherein the metal silicide is characterized as cobalt silicide.

40. The method of claim 36wherein the metal silicide is formed over the source/drain region.

41. The method of claim 36 wherein the gate is a gate of a transistor, wherein the metal silicide is a source/drain metal silicide of the transistor.

42. The method of claim 36 wherein the source/drain dopant includes boron.

43. The method of claim 36 wherein the source/drain dopant includes a source/drain extension dopant for forming a source/drain extension in substrate.

44. A method of forming a semiconductor device, the method comprising:
forming a gate over a silicon semiconductor substrate;
implanting particles including germanium into a region of the substrate after the forming the gate;
activating the germanium implanted into the region;
implanting a source/drain dopant into the substrate for forming at least a portion of a source/drain region in the substrate, wherein the implanting the source/drain dopant is performed subsequent to the activating the germanium;
forming a nickel silicide over the region after the activating.

45. In a transistor device structure having a gate stack and source/drain contact regions comprised primarily of a first material, wherein the source/drain contact regions have a lattice constant, a method of forming a contact, comprising:

implanting particles including atoms having an atomic radius larger than an atomic radius of the atoms of the first material into source/drain contact regions;

activating the atoms of the particles implanted into the source/drain contact regions to increase the lattice constant of the source/drain contact regions;

forming a metal silicide over the source/drain contact regions after the activating of the atoms.

46. The method of claim 45, further comprising doping the source/drain contact regions with P-type material after activating the atoms and prior to forming the metal silicide.

47. The method of claim 46, wherein the first material comprises silicon, the atoms comprise germanium, and the metal silicide comprises nickel silicide.